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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,633	07/13/2001	Kelly T. Hurley	2000-0100.00	3692

7590 07/23/2003

David J. Paul
Agent for Applicant
Micron Technology, Inc.
8000 S. Federal Way, MS 525
Boise, ID 83716

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,633	HURLEY, KELLY T.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-10 and 20 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishioka et al. (U.S. Patent 5,994,733).

Nishioka discloses a method for forming a flash memory device in a semiconductor assembly, comprising the steps of (See col. 11, line 40 to col. 12, line 22 and FIG. 2B):

forming a series of floating gate devices (FIG. 2B, 7) having their source electrodes connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode;

forming a metal interconnect running a major length of the connected together source electrodes, the metal interconnect making a substantially continuous contact

therebetween and spanning completely between neighboring gate electrodes (FIG. 2B); and

forming a metal drain plug (FIG. 2B, 20a) for each floating gate device (FIG. 2B, 7) of the series of floating gate devices, the metal drain plug connecting between a drain electrode of each floating gate device and a digit line (FIG. 2B, 20b) and self-aligning the metal drain plug to respective drain electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 7-10, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al. (U.S. Patent 5,994,733) in view of Watanabe et al. (IEDM, 98 pp. 975-978).

Nishioka discloses a method for forming a flash memory device in a semiconductor assembly, comprising the steps of (See col. 11, line 40 to col. 12, line 22 and FIG. 2B):

forming a series of floating gate devices (FIG. 2B, 7) having their source electrodes connected together by a conductive doped active area, the source electrodes being self-aligned to their respective gate device;

forming a planarized insulation layer (FIG. 2B, 16) over the memory transistors;

removing portions of the planarized insulation layer to self-align an interconnect via to the source electrodes (FIG. 2B);

forming a metal interconnect into the interconnect via, the metal interconnect running a major length of the connected together source electrodes and making contact therebetween and spanning completely between neighboring gate electrodes (FIG. 2B); and

forming a metal drain plug (FIG. 2B, 20a) for each floating gate device (FIG. 2B, 7) of the series of floating gate devices, the metal drain plug self-aligned to and connected between a drain electrode of each floating gate device and a digit line (FIG. 2B, 20b) and self-aligning the metal drain plug to respective drain electrode.

Nishioka fails to disclose forming a nitride barrier layer overlying each transistor gate and a planarized insulation layer over the nitride barrier layer then removing portions of the planarized insulation layer while using the nitride barrier layer to self-align an interconnect via to said source electrodes and wherein the interconnect and drain plug comprises tungsten-base (W).

Watanabe disclose forming a nitride barrier layer overlying each transistor gate and a planarized insulation layer over the nitride barrier layer then removing portions of the planarized insulation layer while using the nitride barrier layer to self-align an interconnect via to the source electrodes and wherein the interconnect and drain plug comprises tungsten-base (W) (pp. 975-976 and FIGS. 1(a-b) to 2(a-b)). Watanabe also discloses forming a tungsten-based interconnect into the interconnect via, the tungsten-based interconnect running a major length of the connected together source electrodes

and making contact therebetween and spanning completely between neighboring gate electrodes (FIG. 2a). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Nishioka and Watanabe to enable the nitride barrier layer, tungsten-based interconnect, and tungsten-based drain plug of Nishioka to be formed and furthermore to obtain a high density flash memory (Abstract).

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-10 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
July 3, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800